FIG. 1A

DYNAMICALLY ADJUSTABLE DIGITAL GYRATOR HAVING EXTENDED FEEDBACK

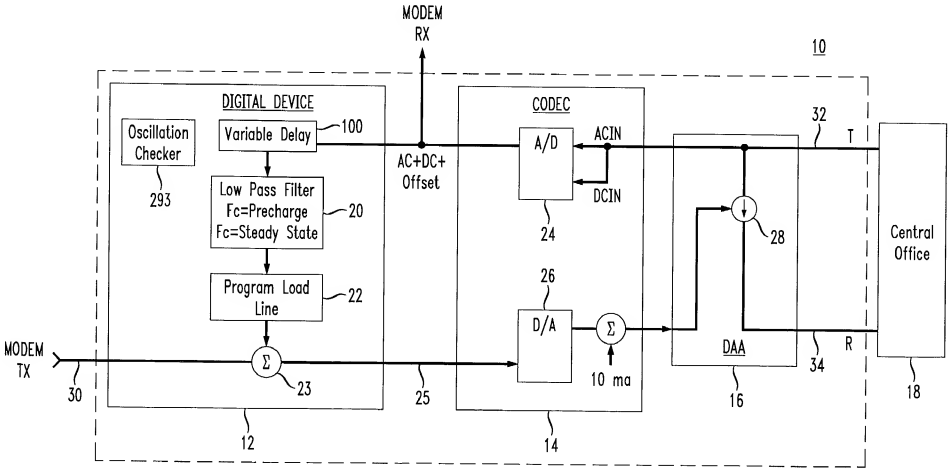


FIG. 1B

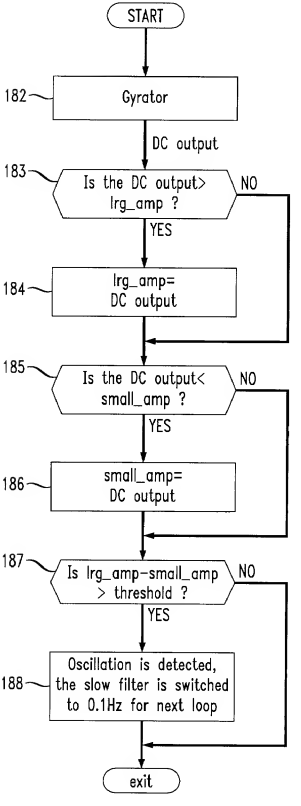
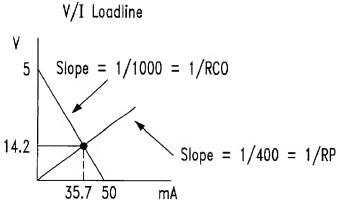

START
182
Gyrator
DC output
183
Is the DC output> Irg_amp ?
NO
YES
184
Irg_amp= DC output
185
Is the DC output< small_amp ?
NO
YES
186
small_amp= DC output
187
Is Irg_amp-small_amp > threshold ?
NO
YES
188
Oscillation is detected, the slow filter is switched to 0.1Hz for next loop
exit

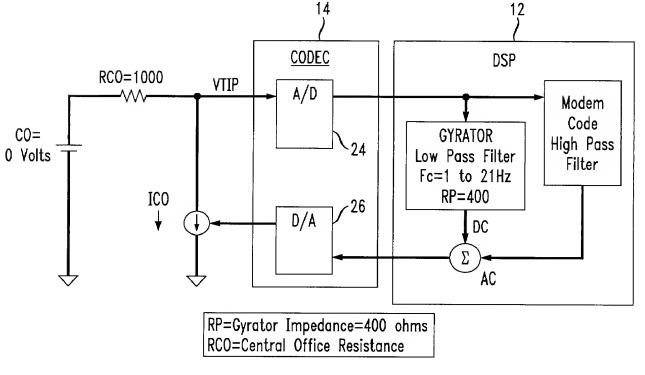
FIG. 2A



50-ICO*RCO=ICO*RP=VP
ICO=14.27 mA
VP=35.7 Volts
Note: All results are at steady state

FIG. 2B

DYNAMICALLY ADJUSTABLE DIGITAL GYRATOR EXAMPLE



RP=Gyrator Impedance=400 ohms
RCO=Central Office Resistance

FIG. 3A

CODEC and Telephone System Stability Block Diagram

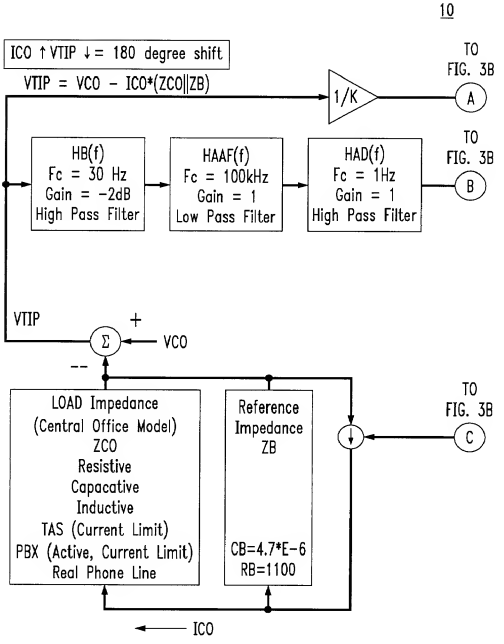


FIG. 3B

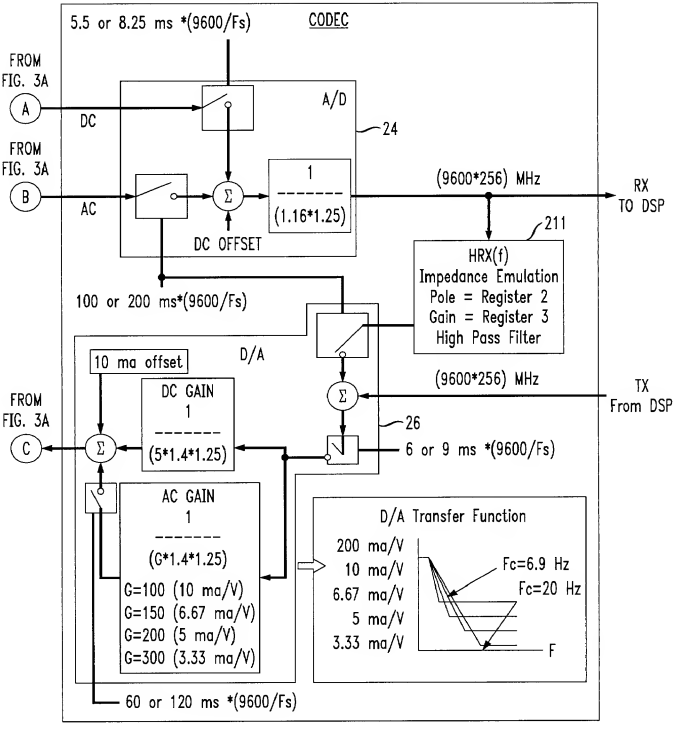

5.5 or 8.25 ms *(9600/Fs)
CODEC
FROM FIG. 3A
A
DC
A/D
24
FROM FIG. 3A
B
AC
1
(1.16*1.25)
(9600*256) MHz
RX TO DSP
DC OFFSET
211
HRX(f)
Impedance Emulation
Pole = Register 2
Gain = Register 3
High Pass Filter
100 or 200 ms*(9600/Fs)
10 ma offset
D/A
(9600*256) MHz
TX From DSP
FROM FIG. 3A
C
DC GAIN
1
(5*1.4*1.25)
26
6 or 9 ms *(9600/Fs)
AC GAIN
1
(C*1.4*1.25)
G=100 (10 ma/V)
G=150 (6.67 ma/V)
G=200 (5 ma/V)
G=300 (3.33 ma/V)
D/A Transfer Function
200 ma/V
10 ma/V
6.67 ma/V
5 ma/V
3.33 ma/V
Fc=6.9 Hz
Fc=20 Hz
F
60 or 120 ms *(9600/Fs)

FIG. 4

Simplified D/A Path

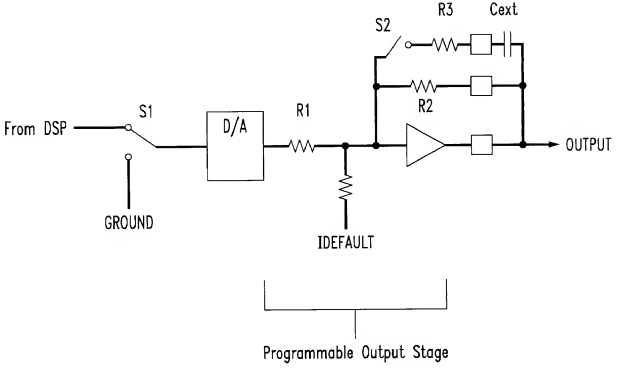


FIG. 5A

DSP Based Gyrator Block Diagram

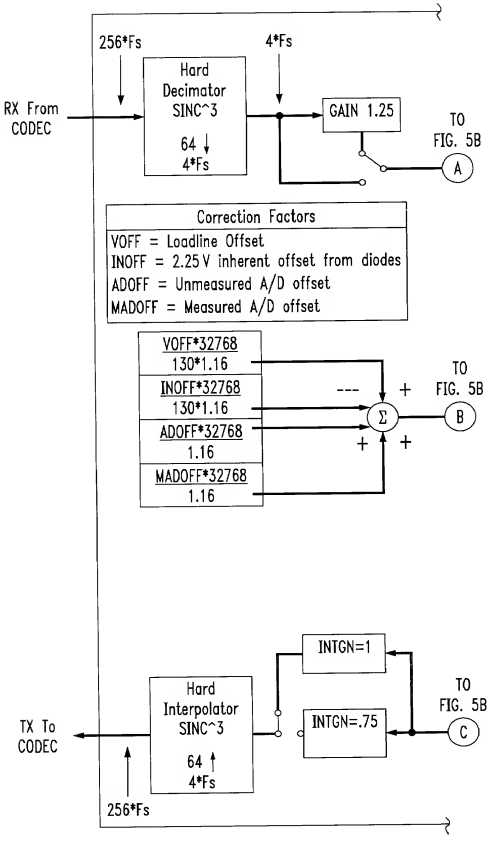
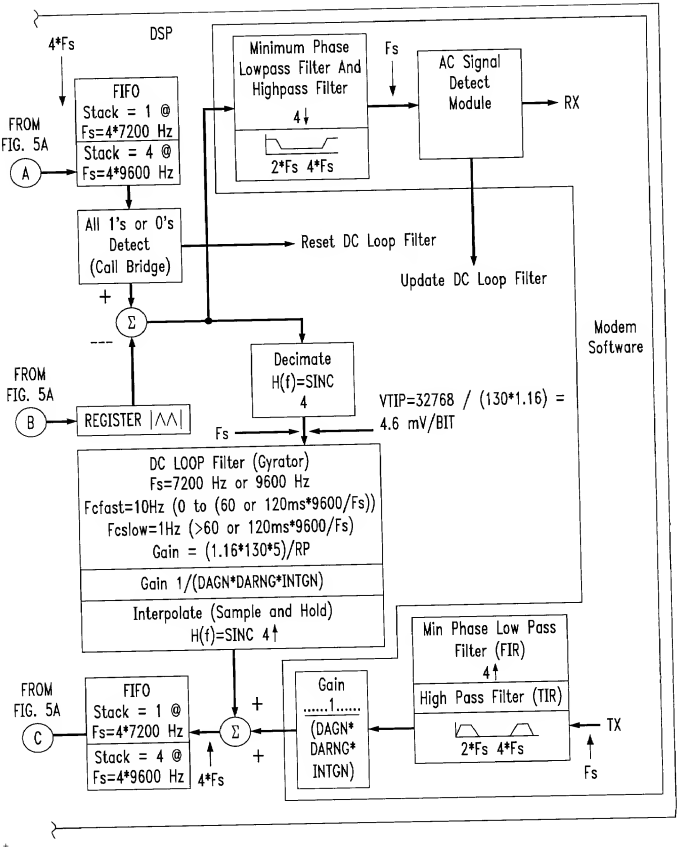
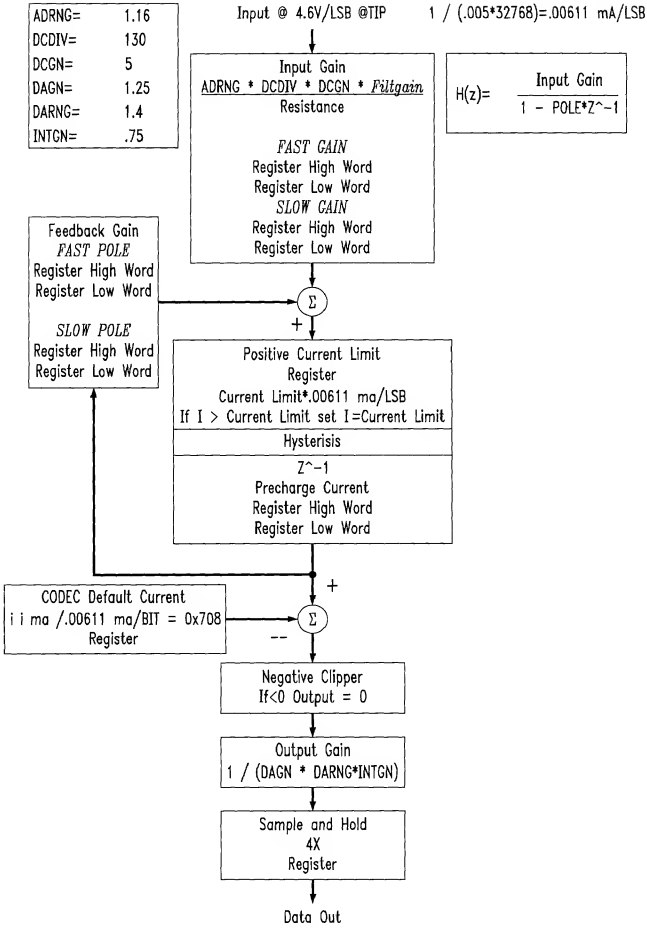


FIG. 5B


DSP
4*Fs
FIFO
Stack = 1 @
Fs=4*7200 Hz
Stack = 4 @
Fs=4*9600 Hz
FROM
FIG. 5A
A
Minimum Phase
Lowpass Filter And
Highpass Filter
4↓
2*Fs 4*Fs
Fs
AC Signal
Detect
Module
RX
All 1's or 0's
Detect
(Call Bridge)
Reset DC Loop Filter
Update DC Loop Filter
Modem
Software
+
Σ

FROM
FIG. 5A
B
REGISTER |∧∧|
Decimate
H(f)=SINC
4
VTIP=32768 / (130*1.16) =
4.6 mV/BIT
Fs
DC LOOP Filter (Gyrator)
Fs=7200 Hz or 9600 Hz
Fcfast=10Hz (0 to (60 or 120ms*9600/Fs))
Fcslow=1Hz (>60 or 120ms*9600/Fs)
Gain = (1.16*130*5)/RP
Gain 1/(DAGN*DARNG*INTGN)
Interpolate (Sample and Hold)
H(f)=SINC 4↑
Min Phase Low Pass
Filter (FIR)
4↑
High Pass Filter (TIR)
2*Fs 4*Fs
TX
Fs
Gain
.....1.....
(DAGN*
DARNG*
INTGN)
FROM
FIG. 5A
C
FIFO
Stack = 1 @
Fs=4*7200 Hz
Stack = 4 @
Fs=4*9600 Hz
4*Fs

FIG. 6


ADRNG= 1.16
DCDIV= 130
DCGN= 5
DAGN= 1.25
DARNG= 1.4
INTGN= .75
Input @ 4.6V/LSB @TIP
1 / (.005*32768)=.00611 mA/LSB
Input Gain
ADRNG * DCDIV * DCGN * Filtgain
Resistance
FAST GAIN
Register High Word
Register Low Word
SLOW GAIN
Register High Word
Register Low Word
H(z)= Input Gain / 1 - POLE*Z^-1
Feedback Gain
FAST POLE
Register High Word
Register Low Word
SLOW POLE
Register High Word
Register Low Word
Σ
+
Positive Current Limit
Register
Current Limit*.00611 ma/LSB
If I > Current Limit set I=Current Limit
Hysterisis
Z^-1
Precharge Current
Register High Word
Register Low Word
+
CODEC Default Current
i i ma /.00611 ma/BIT = 0x708
Register
Σ
--
Negative Clipper
If<0 Output = 0
Output Gain
1 / (DAGN * DARNG*INTGN)
Sample and Hold
4X
Register
Data Out

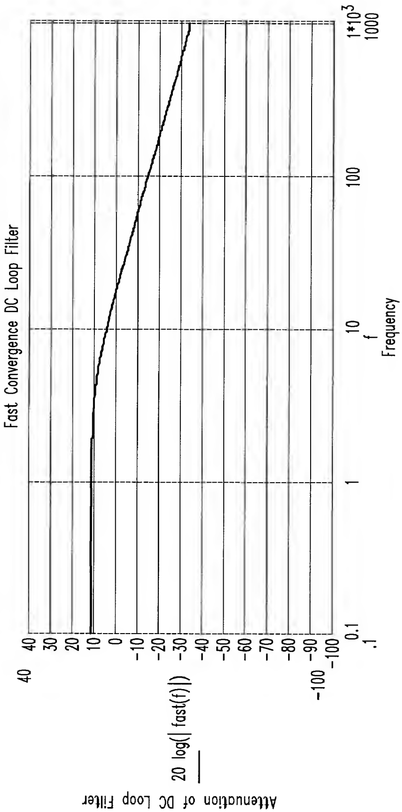

Fast Convergence DC Loop Filter
40
30
20
10
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
40
20 log(|fast(f)|)
−100
Attenuation of DC Loop Filter
0.1
.1
1
10
100
1*10^3
1000
f
Frequency

FIG. 7A

FIG. 7B

10 Hz Fast DC Loop Filter Gain and Phase

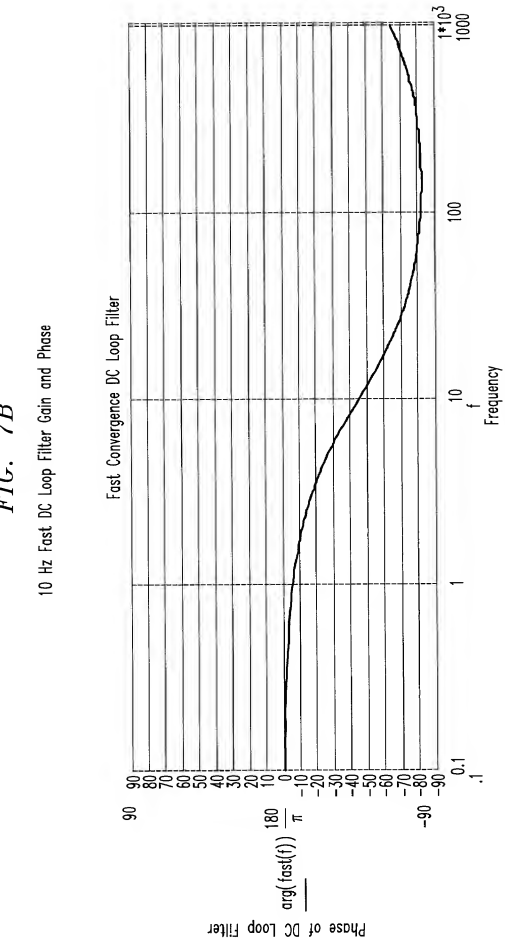


FIG. 8A

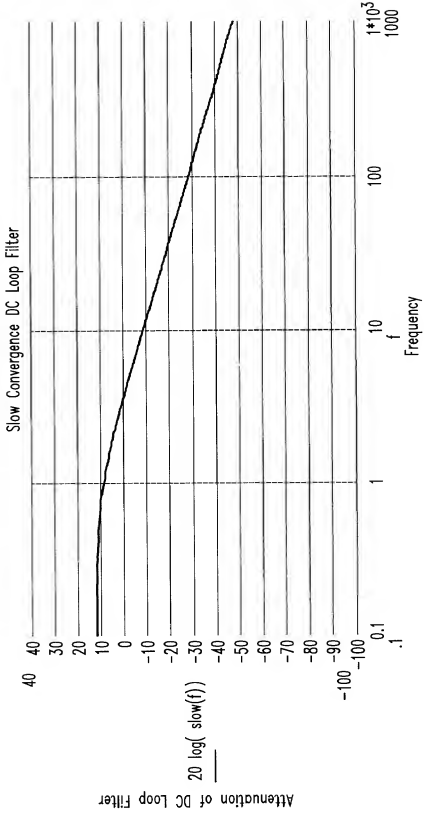

Slow Convergence DC Loop Filter
Attenuation of DC Loop Filter
20 log(slow(f))
40
30
20
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-100
0.1
.1
1
10
f
Frequency
100
1*10^3
1000

FIG. 8B

1 Hz Slow DC Loop Filter Gain and Phase

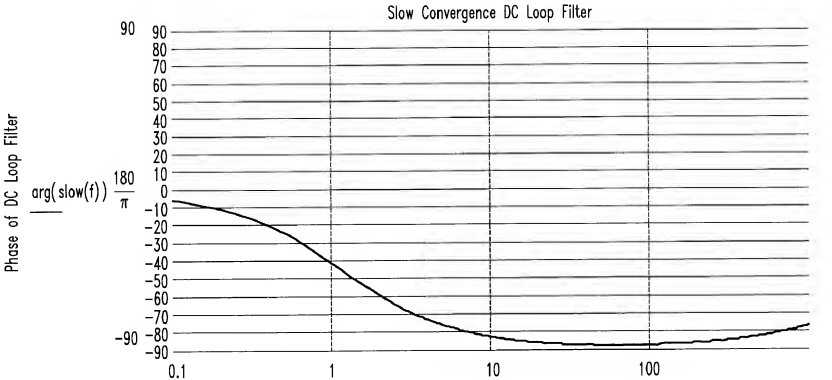


FIG. 9

First Order Filter Topology

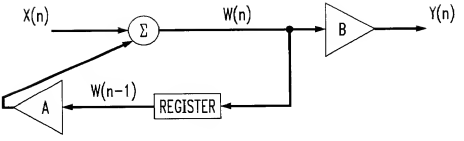


FIG. 10

Final Low Pass Topology with glitch removed

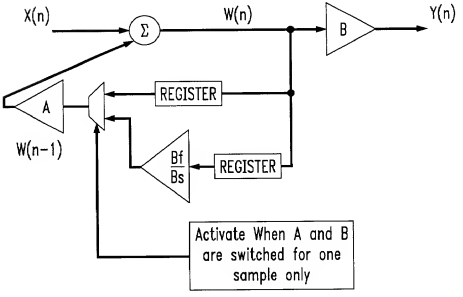


FIG. 11A

DC Loop Filter Without Hysterysis

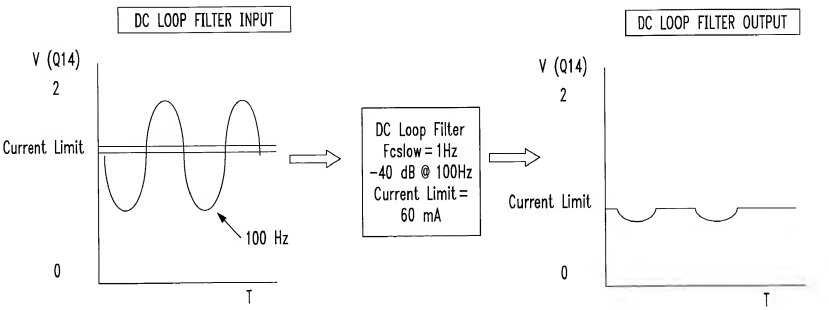


FIG. 11B

DC Loop Filter With Hysterysis

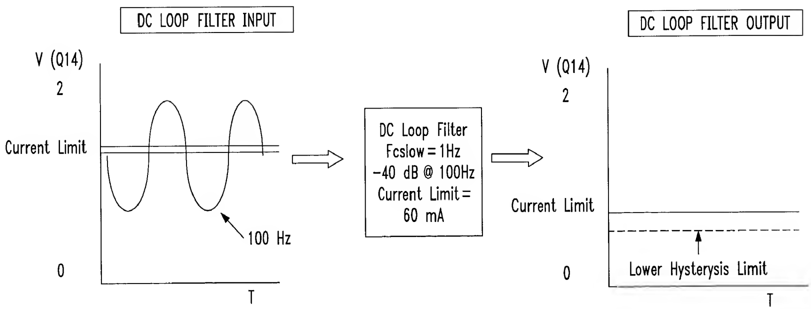


FIG. 12A

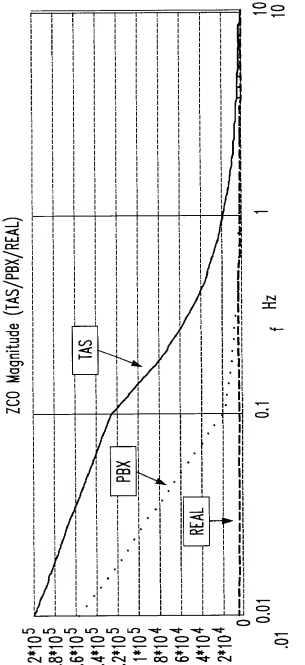


FIG. 12B

TAS, PBX and Real Phone Line V/I Loadlines

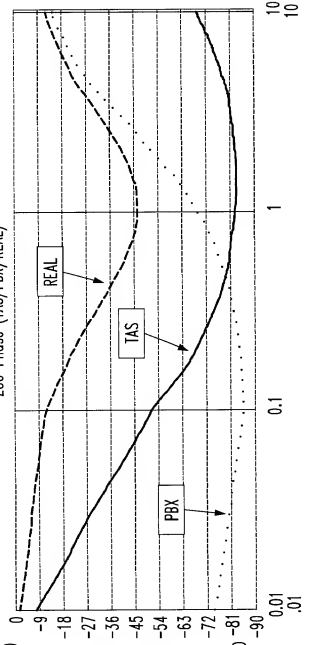


FIG. 13A

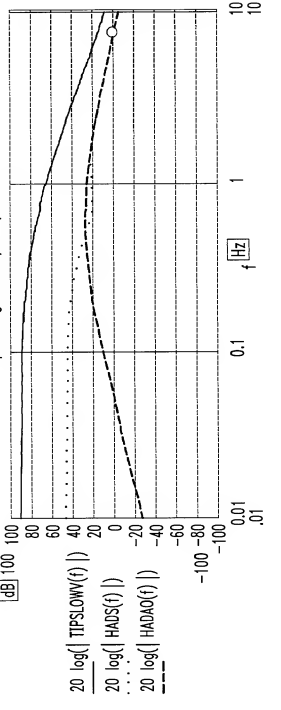


FIG. 13B

TAS Termination with Lowpass Filter Cutoff = 1 Hz

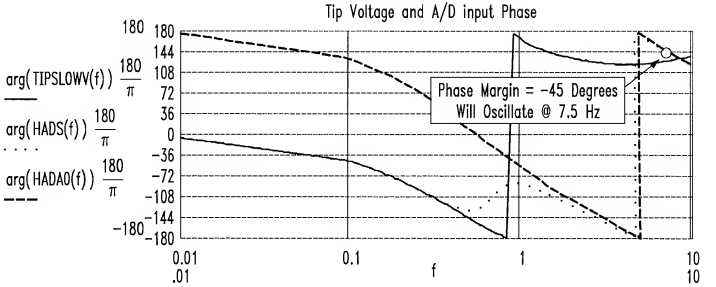


FIG. 14A

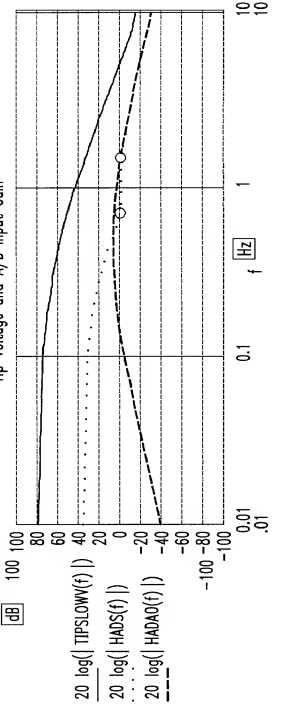


FIG. 14B

TAS Termination with Lowpass Filter Cutoff = .1 Hz

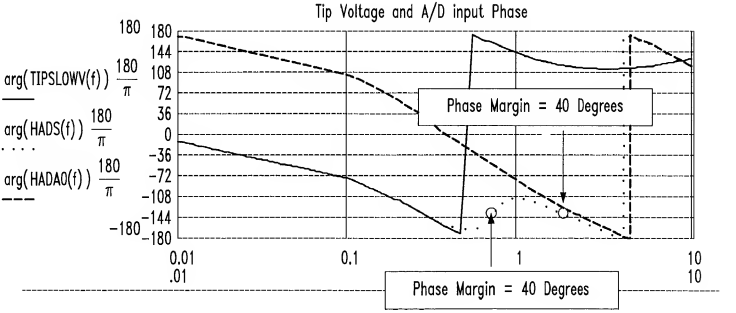


FIG. 15
PRIOR ART

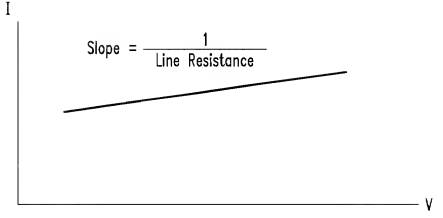


FIG. 16
PRIOR ART

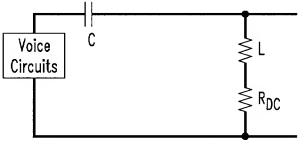


FIG. 17
PRIOR ART

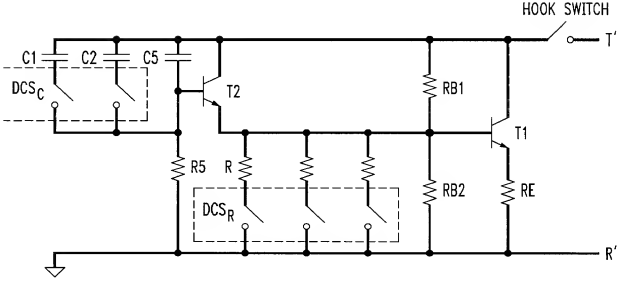
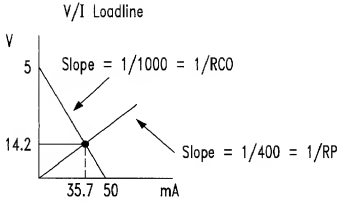


FIG. 18A
PRIOR ART



50-ICO*RCO=ICO*RP=VTIP
ICO=14.27 mA
VP=35.7 Volts
Note: All results are at steady state

FIG. 18B
PRIOR ART